Polytechnic
UNIVERSITY

CMOS Current Comparator for RF Dc-Dc Converter Controllers

Lessing Luu, Columbia University
Project Advisors:
Dariusz Czarkowski, James Masciotti, Polytechnic University

November 2002

WICAT TR 02-007

Table of Content

Table of Figures

1.0 Abstract

The increasing demand for high-speed and low-power applications, such as mobile wireless communication devices, has led to a rising interest in current-mode circuits. With its higher speed and lower supply voltage, the current-mode technology appears to be a viable alternative to the voltage-mode. As an important component of analog current-mode signal processing circuit, the continuous-time CMOS current comparator can be used to implement pulse width modulation (PWM). One such circuit is a feedback VLSI controller for RF dc-dc converters, which can be used to decrease the power demand from a power amplifier in a mobile device. The addition of this component into a transmitter will minimize power consumption by dynamically adjusting the supply voltage to the desired value, reducing the average power drawn from the battery, and, thus, prolonging the battery life for mobile wireless communication devices. For the circuit to be effective, the current comparator must exhibit high speed, low dc offset, and low power consumption. During this research, various designs were conceived and numerous simulations were performed in order to find the optimal solution. The final design of the current comparator consists of a current amplifier attached to an inverter, followed by a positive feedback output stage, and two additional inverters.

2.0 Project Description

The overall objective of the research project is to minimize power consumption in mobile wireless communication devices. A power consuming component of such devices is the power amplifier. Adding a RF dc-dc converter into it will minimize the power consumed but will also require a converter controller. The focus of this particular project is to design a specific component in the converter controller, namely, an analogue integrated circuit building block called a current comparator.

Unlike digital circuits where minimizing the size of the technology will inevitably optimize the functionality of a circuit, analog circuits do not necessarily share such a direct relationship. In other words, working with the smallest available technology does not guarantee an optimal circuit. Since the project is a component of a RF dc-dc converter controller [1] that used 0.5um CMOS technology, it is natural to begin designing the current comparator with the same technology.

The final performance of the 0.5um CMOS current comparator satisfies the general specifications required for the converter controller to be of practical use; the converter controller can also be fabricated on one integrated circuit, as opposed to two, using the same technology. On the other hand, this current comparator did not perform as well as some of the other existing designs that used different technologies. Thus, the goal of the latter part of the research was to design a current comparator that exhibits the best performance to date. If the results are significantly better than the 0.5um CMOS current comparator, then fabricating the controller with two integrated circuits using different technologies may be a viable alternative. 0.25um

CMOS technology was used for this part of the research. In both instances, the design methodology and the general schematics are very similar.

3.0 Transceivers

All mobile wireless communication devices come with a transceiver, which is a component that transmit and receive signals. In such devices, the transceivers generally consume more power than any of the computer parts. The power amplifier (one of the functional blocks in the transceiver) consumes more than 50 % of the power. In other words, this functional block alone consumes more power than all the other functional blocks combined. Therefore, reducing the power consumed in the power amplifier will greatly decrease the overall power of the device. Data sheets of power consumption of each of the functional blocks can be obtained [2].

3.1 Power Amplifier

A power amplifier uses a Class AB output stage (Figure 1) because of its linearity and

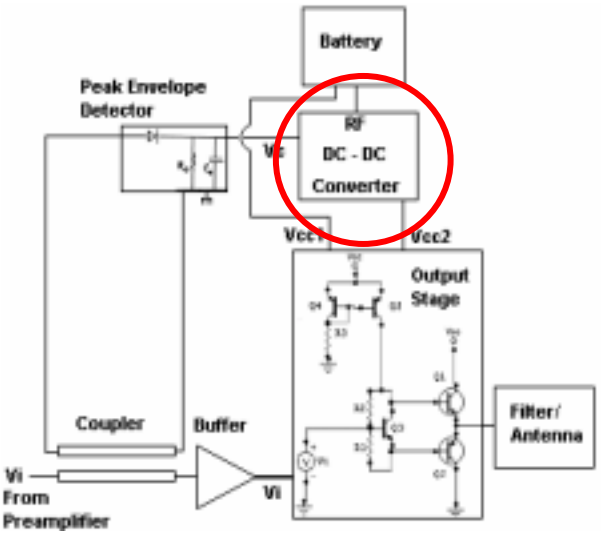


Figure 1: Power Amplifier with RF DC-DC Converter

power efficiency. For the output stage to achieve its maximum efficiency of 78 %, the input fed into the output stage must be the maximum level amplitude of the input signal, which is referred to as the envelope of the signal. Having the battery directly feed into the input will not achieve this efficiency. However, by adding a RF dc-dc converter that follows the peak envelope of the input signal and using it to power the output stage (Figure 1), it can theoretically operate at a constant maximum efficiency of 78 %.

One must also account for the power consumed by the additional components added into the power amplifier, such as the converter and the converter controller. However, by designing these components to consume minimal power relative to the power amplifier, much power can be saved.

3.1.1 RF Dc-Dc Converter

A radio frequency (RF) dc-dc converter can quickly change a constant dc voltage to a different voltage. This requires the converter to take in a pulse as its input, and depending on the widths of the pulses (duty ratio), it can adjust the output voltage accordingly.

There are several types of converters. A Buck converter only produces voltages that are greater than the battery voltage. A Boost converter only produces voltages that are less than the battery voltage. To follow a peak envelope of the input signal in a power amplifier, a very fast bi-directional converter (can convert above and below the battery voltage) is necessary. Such a fast converter was designed by the authors of [3].

3.1.2 RF Dc-Dc Converter Controller

To operate a RF dc-dc converter, a converter controller must feed in modulated pulse widths into the converter input before the voltages can be changed to a different value. The act of changing pulse widths is referred to as pulse width modulation (PWM). Converter controllers are governed by Control Laws, which are described in great length [4].

A current mode feed-forward controller for a buck converter is illustrated below (Figure 2). For more examples, refer to [1]. The primary current-mode components of a controller those these topologies are current conveyors (CCII) and current comparators (circled below), as shown. This research project is focused on designing a fast current comparator for a RF dc-dc converter controller.

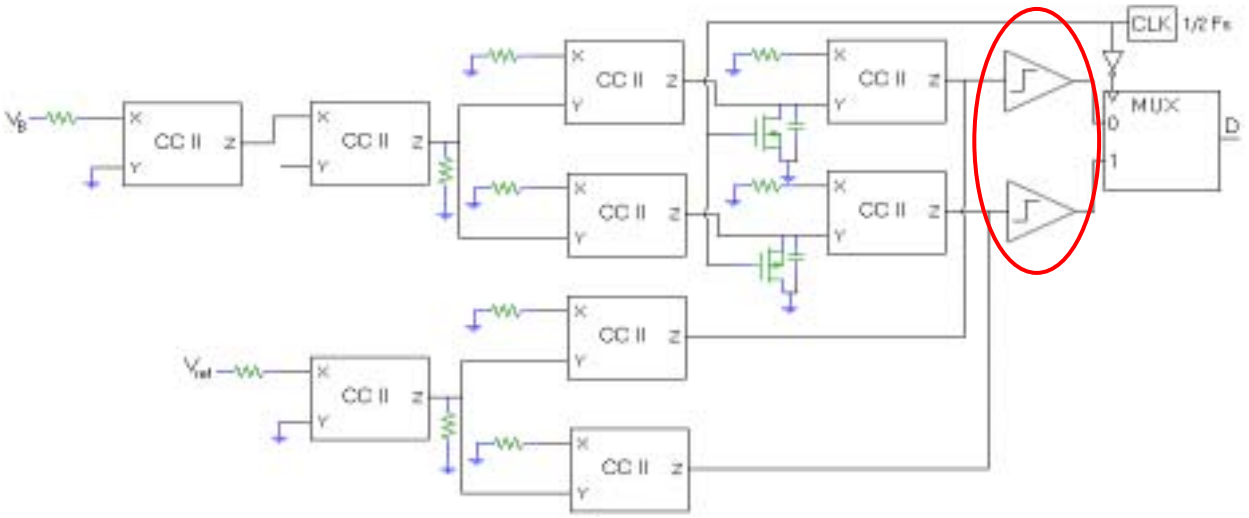


Figure 2: Current Mode Feed-Forward Controller for A Buck Converter

4.0 Current Comparator

A current comparator is an analog current-mode signal processing circuit. The functionality of this continuous-time component is quite basic: it takes a current as input and outputs a voltage (Figure 3). A positive current (current going into the circuit) results in $+V_{dd}$ output, whereas a negative current (current going out of the circuit) results in $-V_{dd}$ output (Figure 4).

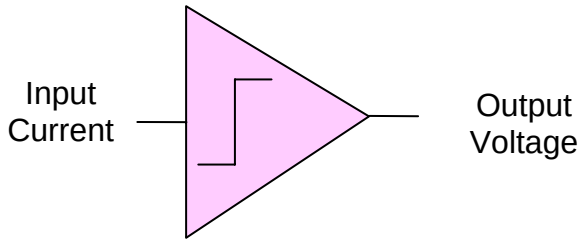


Figure 3: Symbol View of Current Comparator

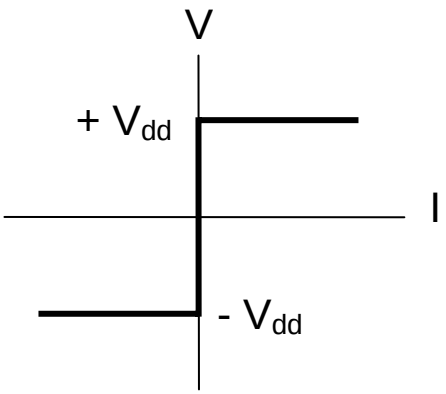


Figure 4: Characteristic of Current Comparator

The difficulty in designing a current comparator, as with designing any circuit, is to have the actual circuit emulate the ideal characteristics of the circuit as much as possible.

Various current comparators have been proposed [5] and [6]. The design of the current comparator to be used is a modified version of the original simple current comparator [5].

4.1 Important Considerations

There are important considerations to keep in mind when designing a current comparator. Given that the converter controller, in which the current comparator will be used, will be controlling a very fast converter, such as in [3], it is crucial for the circuit to exhibit high speed through its ability to switch very quickly. Another consideration is to have the switching take place when the input current is as close to zero as possible, also referred to as a low dc offset. This will ensure that the current comparator does not misread a positive current as being negative and vice versa. Lastly, the circuit must exhibit low power consumption, since the purpose of the project is to minimize the power consumed in a power amplifier. Adding a high power consuming current comparator is not practical.

The general design methodology is to apply these important considerations to the individual components of the current comparator. The rationale behind this methodology is that individual well-behaved components assembled together should maintain a well-behaved performance. Although this is not always necessarily the case, it is a sufficient basis to start the design process.

After designing each component of the current comparator and assembling them together, additional adjustments were made to optimize the overall performance of the circuit.

4.2 Components

The final current comparator consists of a current amplifier attached to an inverter, followed by a positive feedback output stage, and two additional inverters (Figure 5).

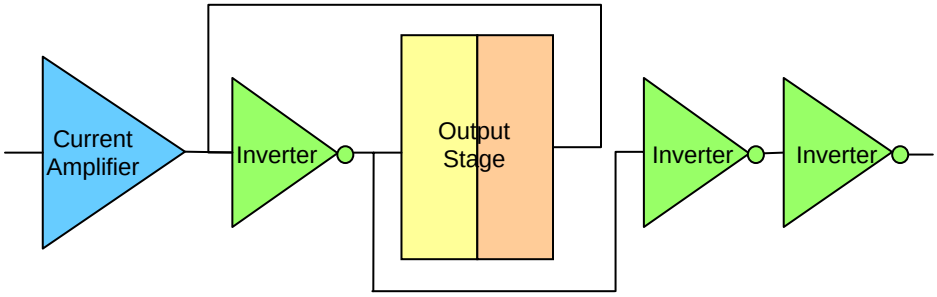


Figure 5: Symbol View of Current Comparator Components

The following section will discuss each individual component's schematic and design methodology, which will generally apply to both technologies used. Any differences will be discussed. The results mentioned will be that of the 0.5um CMOS current comparator.

4.2.1 Current Amplifier

The original simple current comparator [5] is unable to switch at small currents, making a current amplifier necessary at the input. A current amplifier consists of two current mirrors (Figure 6), which basically reflect the current from input to output. Current mirrors work as follows: the PMOS's have the same gate-to-source voltage (V_{gs}) and the NMOS's have the same gate-to-source voltage (V_{gs}), and since the PMOS's and NMOS's are tied to the highest and lowest voltage potential, respectively, there is no body effect, meaning that the threshold voltage (V_t) is fairly constant. Assuming infinite output resistance and no channel-length modulation for the moment, the drain current (I_d) in saturation mode only depends on width per length of the transistor (W/L). In other words, one can effectively amplify the input current by adjusting W/L of the second set of transistors (M3 and M4) to be larger in magnitude than W/L of the first set of transistors (M1 and M2). The ratio $(W_2/L_2) / (W_1/L_1)$ thus becomes the theoretical gain of the current amplifier.

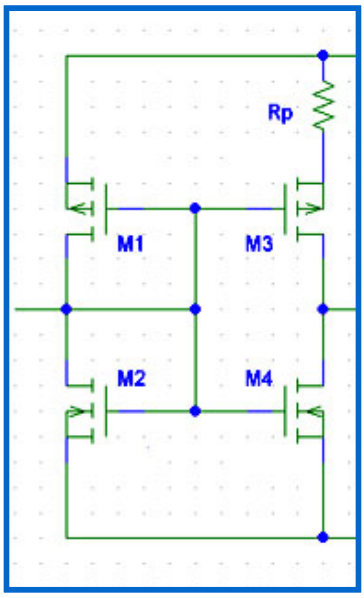


Figure 6: Schematic View of Current Amplifier

In reality, however, the circuit is affected by a finite output resistance, channel-length modulation, and other non-idealities, hence the additional resistor, R_p, to minimize the current offset. The theoretical gain of the current amplifier also differs from the actual gain of the circuit.

The initial rationale when sizing the transistors was to minimize their lengths in order to minimize the effects of channel-length modulation. With lengths kept to a minimum, it is

necessary to adjust the widths and use fairly large values to obtain the desired gain for the current amplifier. However, it was later shown through simulation that the power consumption of this component was unacceptably high due to the large current drive from the large widths. To minimize power consumption, the widths were kept to a minimum while the lengths were adjusted accordingly to achieve a current gain. The latter design proved to be a much more efficient alternative.

There exist an inverse relationship between the gain and the 3db frequency of the current amplifier. Therefore, tradeoffs were made to obtain a decent gain and frequency. The result for the current amplifier is a gain of 12.57 db, or 4.25 (Figure 7), 3db frequency of 161 MHz (Figure 7), and a current offset of 1.29nA (Figure 8).

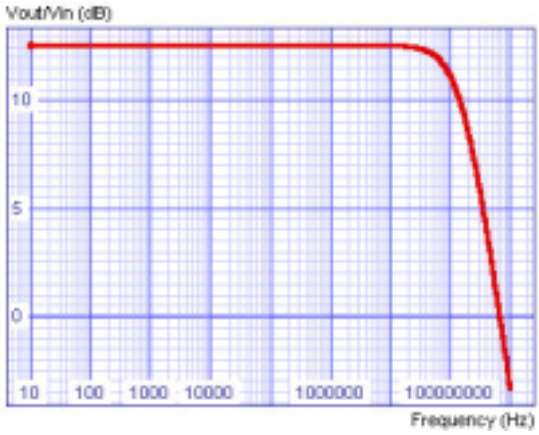


Figure 7: Voltage Transfer Function of Current Amplifier

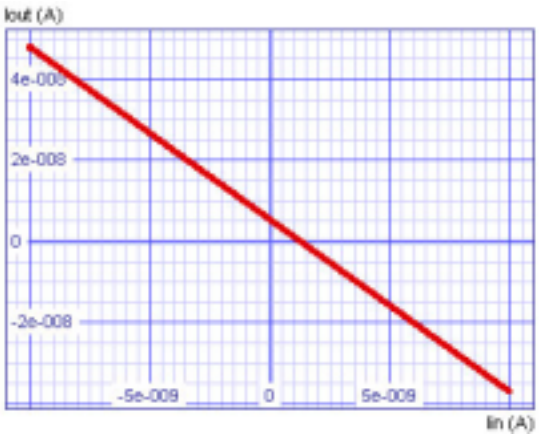


Figure 8: DC Current Offset of Current Amplifier

4.2.2 Inverter

An inverter consists of a PMOS and a NMOS (Figure 9). The current comparator consists of three inverters: one in the positive feedback loop and two at the output to make the output voltage rail-to-rail. A primary concern when designing an inverter is to minimize the voltage offset, which will prevent further delay in the current comparator. It is also important to minimize the area of the gate to reduce parasitic capacitances, but at the same time allow the inverter to draw more current to charge faster. One way of approaching this issue is to minimize the lengths of the transistors and adjust the widths accordingly.

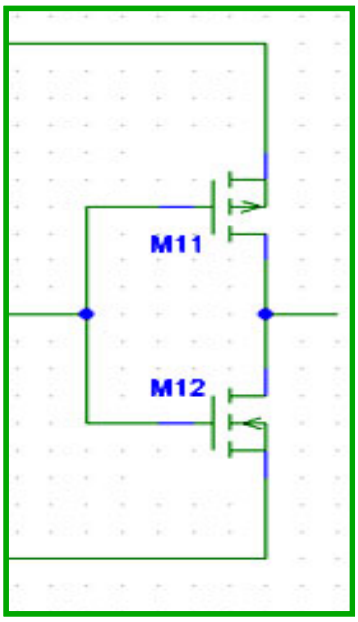


Figure 9: Schematic View of Inverter

The final current comparator has three identically sized inverters. The inverter's transfer characteristic is shown below (Figure 10). The voltage offset of the inverter is 5.5 mV (Figure 11), which is minimal. The delay of the inverter is 32 psec, which is negligible.

Figure 10: Transfer Characteristic of Inverter

Figure 11: DC Voltage Offset of Inverter

4.2.3 Output Stage: Class B

The ideal scenario for the current comparator is to have the input and output voltages of the output stage linearly related. That way, the output stage is not distorting or delaying the input signal. A Class B output stage, which is used in the original simple circuit, consists of a PMOS and a NMOS transistor (Figure 12).

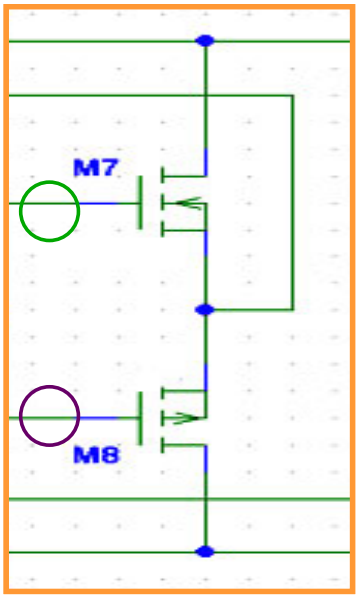


Figure 12: Schematic View of Class B Output Stage

The problem with a Class B output stage is the existence of a dead-band region at low input (Figure 13), which will result in a delay at the output. One way of resolving this problem is to convert the Class B output stage to a Class AB output stage.

Incidentally, when the PMOS and NMOS transistor are sized the same using 0.25um CMOS technology, the dead-band region appears to be negligible, suggesting that it is acceptable to use a Class B output stage. This proposition holds true, from simulation, for this technology. However, the same cannot be said for the output stage using 0.5um CMOS technology, which has a significant dead-band region (Figure 14).

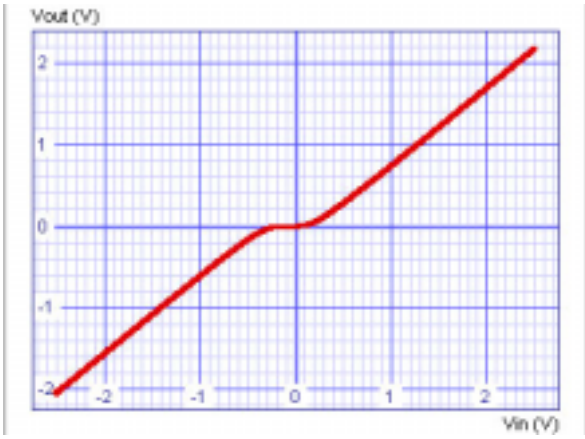


Figure 13: Transfer Characteristic of Class B Output Stage

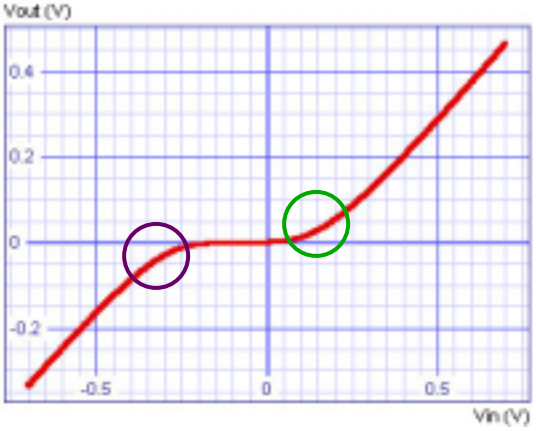


Figure 14: Zoomed-In Transfer Characteristic of Class B Output Stage

4.2.4 Output Stage: Class AB

A Class AB output stage can effectively remove the dead-band region from a Class B output stage. The idea is to individually bias the voltages at the NMOS and PMOS gates, thus "collapsing" the dead-band region.

One approach to this issue was to begin with the same PMOS and NMOS dimensions as the inverter. From there, one can identify the biasing voltages for each gate by approximating the input voltage where the graph becomes linear. Use those voltages to bias the transistors. After linearity is achieved, adjust the final values of the transistors to minimize the current offset.

There are various ways of biasing the voltages. The method for this design involved diode-connected NMOS transistors. This method will adjust the highest and lowest voltage potentials and feed the appropriate values into the gate

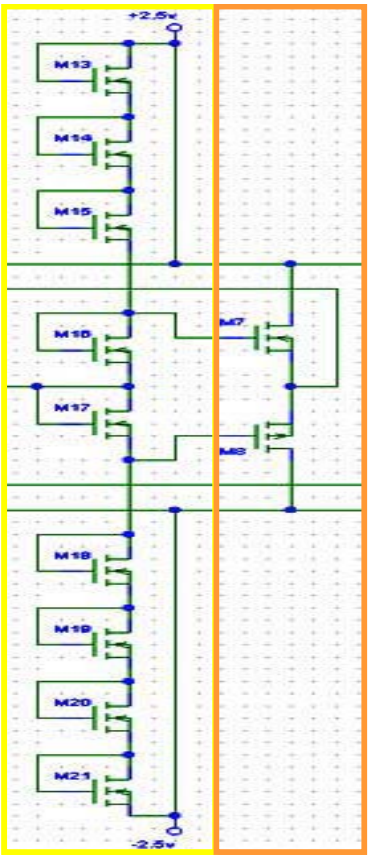


Figure 15: Schematic View of Class AB Output Stage

voltages. The final design required nine such transistors in series (Figure 15).

After appropriate adjustments, the output stage produced a relatively linear graph (Figure 16). The current offset is 2.01 fA (Figure 17), which is negligible.

Figure 16: Transfer Characteristic of Class AB Output Stage

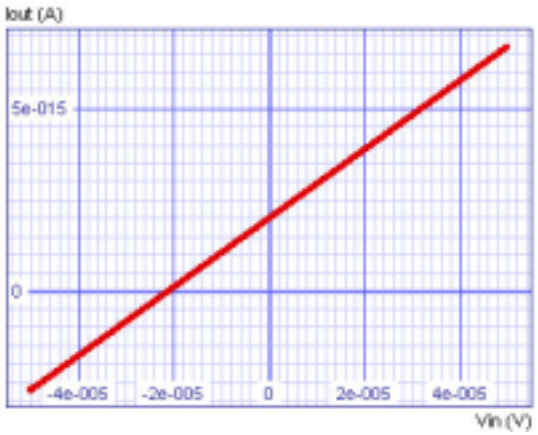


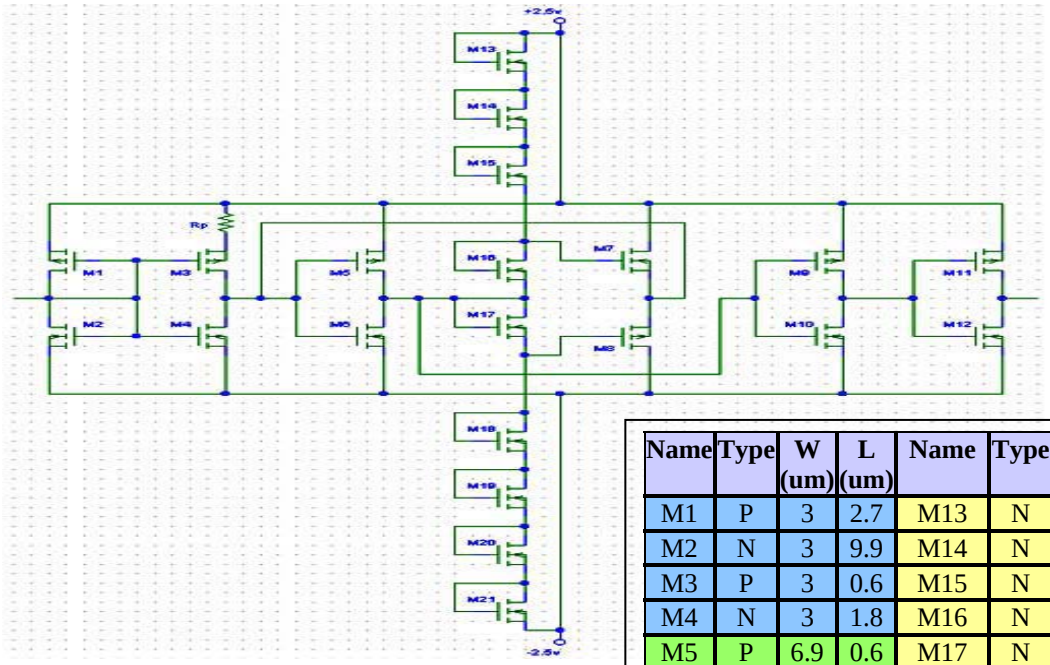
Figure 17: DC Current Offset of Class AB Output Stage

5.0 0.5um CMOS Technology

The RF dc-dc converter controller [1], which the current comparator was intended to be a part of, was designed using 0.5um CMOS technology. The motivation behind using the same technology is to design the converter controller using a single integrated circuit. Below are the results for the current comparator using this technology (Figure 18).

5.1 Circuit Diagram

The final design for the 0.5um CMOS current comparator is shown below (Figure 18). The values for all of the components are also listed.



Name	Type	W (um)	L (um)	Name	Type	W (um)	L (um)
M1	P	3	2.7	M13	N	3	2.1
M2	N	3	9.9	M14	N	3	2.1
M3	P	3	0.6	M15	N	3	2.1
M4	N	3	1.8	M16	N	3	2.1
M5	P	6.9	0.6	M17	N	13.2	0.6
M6	N	3	0.6	M18	N	19.5	0.6
M7	N	3	0.6	M19	N	3	2.1
M8	P	12.6	0.6	M20	N	3	2.1
M9	P	6.9	0.6	M21	N	3	2.1
M10	N	3	0.6	**Voltage**	**Volts**	**Resistor**	**Ohms**
M11	P	6.9	0.6	V +	2.5	Rp	12
M12	N	3	0.6	V -	-2.5		

Figure 18: Schematic View of 0.5um CMOS Current Comparator with Component Values

The technology used is TSMC 0.5um process. The minimum transistor length of the process is 0.6um, lambda is 0.3um, and the maximum supply voltage is 5V. All transistor sizes, thus, are multiples of 0.3um. The minimum transistor width is set at 3um. The positive and negative supply voltages V + and V – were set to 2.5V and -2.5V, respectively.

All the transistors for the current amplifier, M1 to M4, were set to minimum widths to reduce the power consumption of this component, as previously discussed. An additional resistor, Rp, of value 12 Ohms was added to compensate for the non-idealities of the current mirrors in the amplifier. M5 and M6, M9 and M10, and M11 and M12 are the transistors of the three inverters. All of them are dimensioned the same way, with minimum lengths and adjusted widths for a larger current drive. M7 and M8 are the transistors for the output stage, along with the nine diode-connected transistors, which are M13 to M21, used to bias the input gate voltages.

5.2 Simulation Results

The circuit simulator program used for this project is SPICE OPUS. Transistor parameters were obtained from MOSIS Integrated Circuit Fabrication Service [7].

5.2.1 Delay Time

SPICE simulations of the 0.5um CMOS current comparator demonstrated fairly good results. The delay time of this circuit is shown below (Figure 19).

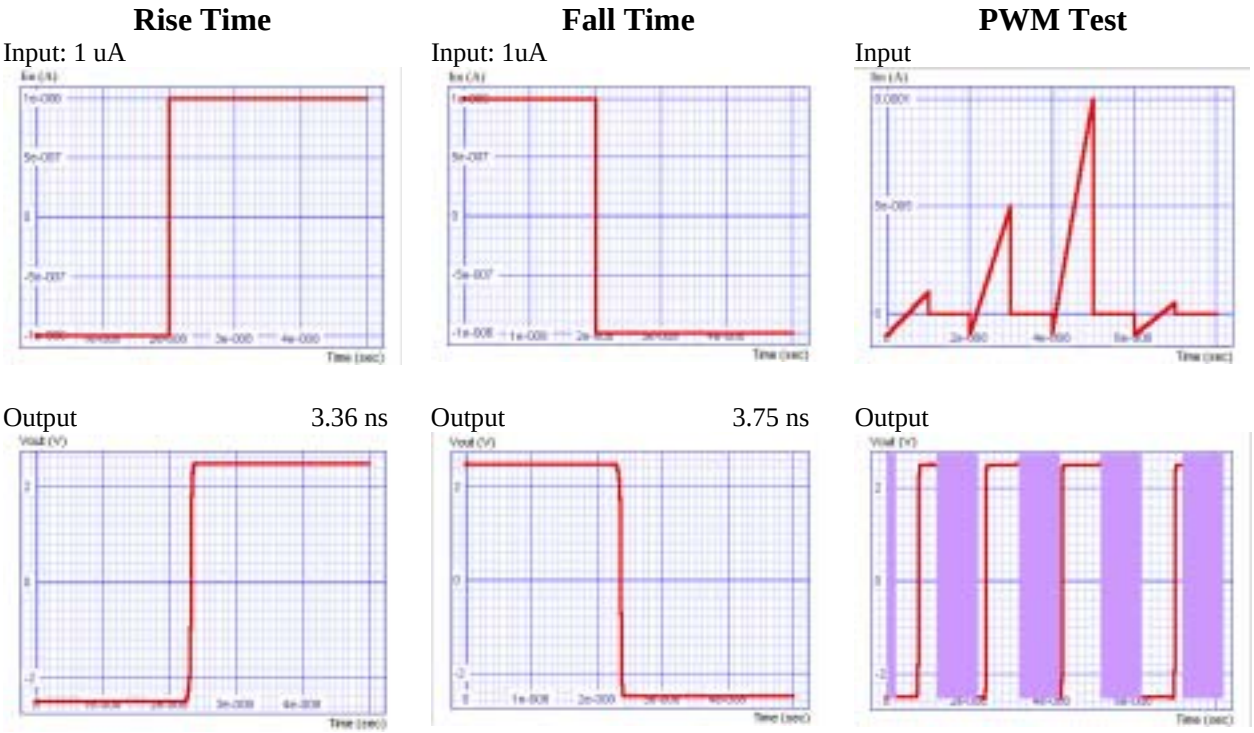


Figure 19: Delay Time of 0.5um CMOS Current Comparator

A current input switching between -1 uA and 1 uA was used to find the delay of the current amplifier. The rise time delay is 3.36 ns and the fall time delay is 3.75 ns. The delay values for

the rise time and fall time were measured when the output voltage (V_{out}) became 2V and -2V, respectively. At this point, the output voltage reaches 90 % of the total peak-to-peak voltage value.

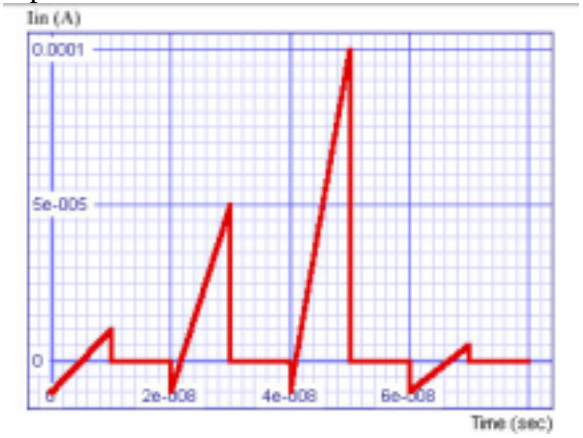
A major concern when simulating the current comparator was to see whether it can switch fast enough at regions where input is low. A large delay for these small signals can jeopardize the performance of the current comparator. For practical measures, an input current with different magnitudes was used to see if the current comparator can output the corresponding duty ratios intended for pulse width modulation. The output graph clearly shows that this current comparator can perform PWM.

The reason for covering up certain regions on the output graph is to only show the parts of the graph that are relevant. Because the converter controller will be switching between two current comparators to provide each one with sufficient time to charge and discharge, those regions covered up are not relevant to the current comparators performance, and hence, not important.

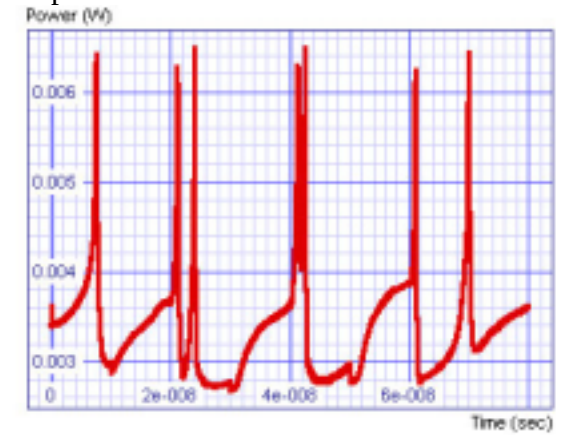
5.2.2 Power Consumption

The power consumption of the current comparator is shown below (Figure 20).

Input



Output: Instantaneous Power



Components	Power (mW)
Current Amplifier: Left	0.150
Current Amplifier: Right	0.733
Inverter 1	1.725
Output Stage: Bias	0.077
Output Stage: Main	0.005
Inverter 2	0.550
Inverter 3	0.060
TOTAL	3.300

Figure 20: Power Consumption of 0.5um CMOS Current Comparator

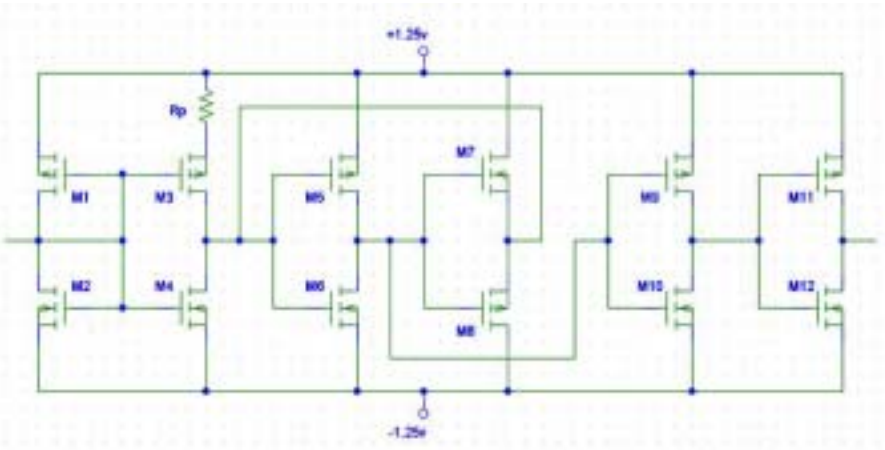
The input current used to measure the power consumption is the same pulse width modulation test current used previously. The graph on the bottom left is the instantaneous power of the given input. The chart on the right summarizes the power consumed by each individual component in the current comparator. The average power consumed is 3.3 mW.

6.0 0.25um CMOS Technology

The results obtained from the 0.5um CMOS current comparator satisfy the criteria for the converter controller specifications. However, the fact that the current comparator did not perform as well as the existing designs created a new motivation to try another technology. Below are the results for the current comparator under this technology.

6.1 Circuit Diagram

The final design for the 0.25um CMOS current comparator is shown below (Figure 21). The values for all of the components are also listed.



Name	Type	W (um)	L (um)
M1	P	0.36	0.48
M2	N	0.36	2.04
M3	P	0.36	0.24
M4	N	0.36	0.6
M5	P	1.08	0.24
M6	N	0.36	0.24
M7	N	0.36	0.24
M8	P	0.36	0.24
M9	P	1.08	0.24
M10	N	0.36	0.24
M11	P	1.08	0.24
M12	N	0.36	0.24
Voltage	**Volts**	**Resistor**	**Ohms**
V +	1.25	Rp	124.9
V -	-1.25		

Figure 21: Schematic View of 0.25um CMOS Current Comparator with Component Values

The technology used is TSMC 0.25um process. The minimum transistor length of the process is 0.25um, lambda is 0.12um, and the maximum supply voltage is 2.5V. All transistor sizes, thus,

are multiples of 0.12um. The minimum transistor width is set at 0.36um. The positive and negative supply voltages V + and V – were set to 1.25V and -1.25V, respectively.

The methodology used to determine the dimensions of the transistors for the current comparator is the very similar to the one used in the 0.5um process. The widths of the current amplifier were kept to a minimum and lengths were adjusted to obtain the desirable gain. The additional resistor, Rp, was also necessary, and its value is 124.9 Ohms. The inverters had minimum length for the same reasons, with all three being the same dimensions as well. However, the output stage, M7 and M8, is significantly different. Because of the small dead-band region for this technology, as previously discussed, a Class B output stage is sufficient. Without the need to bias the gate voltage, the diode-connected transistors used in the 0.5um process are no longer necessary, reducing the total number of transistors from 21 to 12. The result is an output stage with the same dimension for the PMOS and NMOS, both of which have minimum lengths and widths.

6.2 Simulation Results

SPICE simulations of the 0.25um CMOS current comparator demonstrated remarkably good results. The delay time of this circuit is shown below (Figure 22).

6.2.1 Delay Time

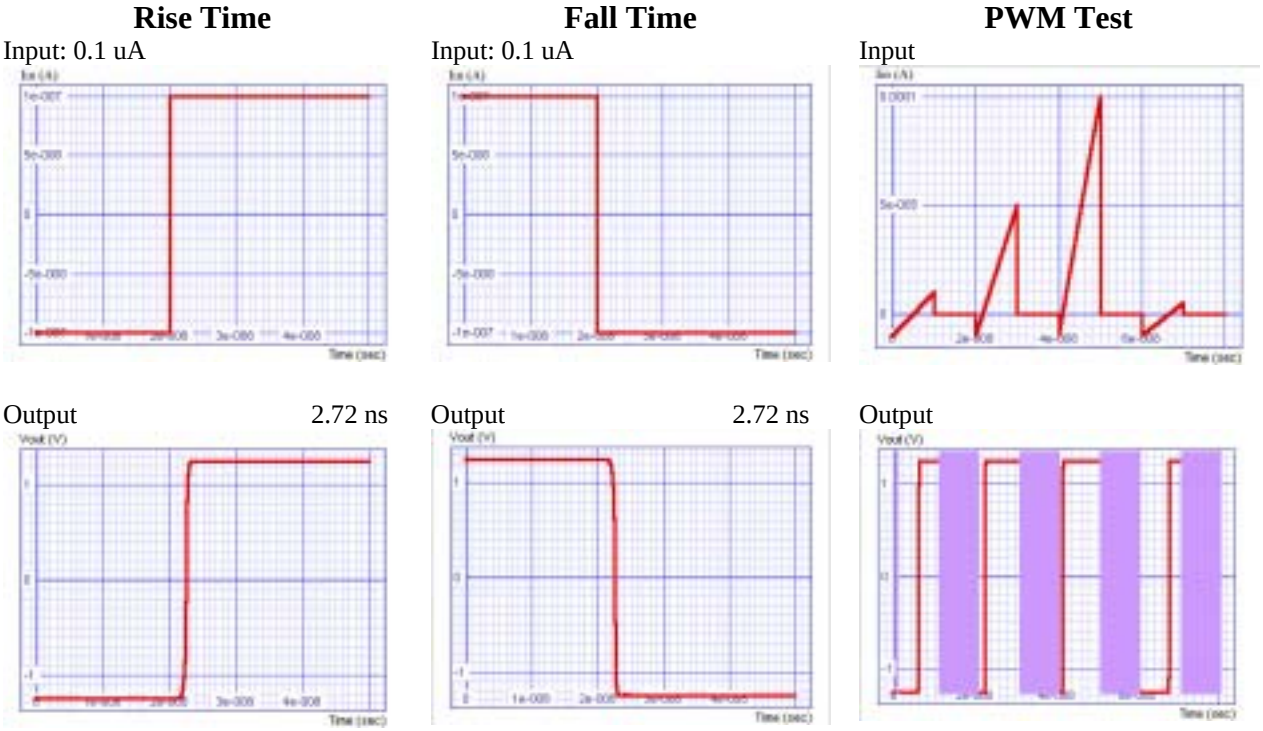


Figure 22: Delay Time of 0.25um CMOS Current Comparator

A current input switching between -0.1 uA and 0.1 uA was used to find the delay of the current amplifier, which is one order of magnitude smaller than the input used in the 0.5um process. Incidentally, the rise time and fall time are both 2.72 ns, which are smaller values in comparison to the previous process despite the smaller input current. The delay values for the rise time and

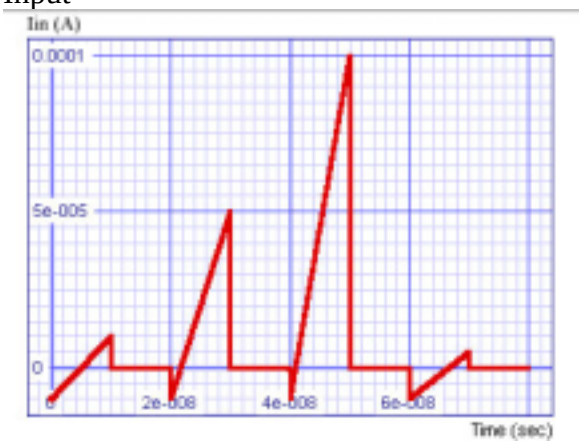
fall time were measured when the output voltage (V_{out}) became 1V and -1V, respectively. At this point, the output voltage reaches 90 % of the total peak-to-peak voltage value.

The same PWM test current was used to see how well this current comparator performs given such a signal. Again, the output graph clearly shows that this current comparator can perform PWM, even with high duty ratios from the input.

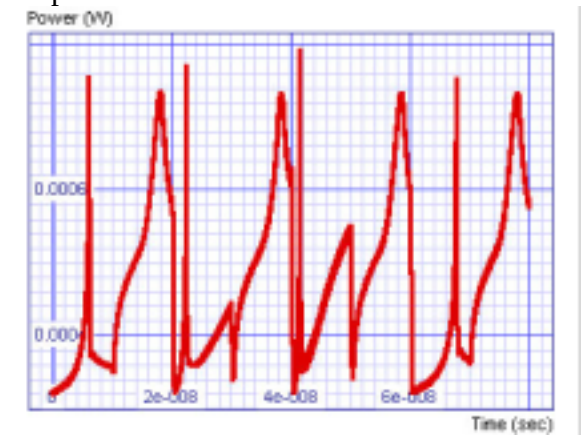
6.2.2 Power Consumption

The power consumption of the current comparator is shown below (Figure 23).

Input



Output: Instantaneous Power



Components	Power (uW)
Current Amplifier: Left	34
Current Amplifier: Right	96
Inverter 1	193
Output Stage: Main	15
Inverter 2	102
Inverter 3	20
TOTAL	460

Figure 23: Power Consumption of 0.25um CMOS Current Comparator

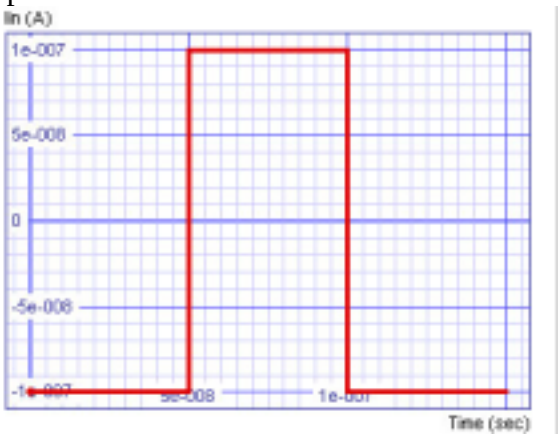
The input current used to measure the power consumption is the same pulse width modulation test current used previously. The graph on the bottom left is the instantaneous power of the given input. The chart on the right summarizes the power consumed by each individual component in the current comparator. The average power consumed is 460 uW, a value significantly smaller than the previous 3.3 mW from the 0.5um process. One of the reasons for

such a considerably large difference in power consumption is due to the smaller total supply voltage, which is half of that in the 0.5um process. The smaller technology also contributed to the reduction in power, since smaller dimensions of the transistors expend less current during each transition.

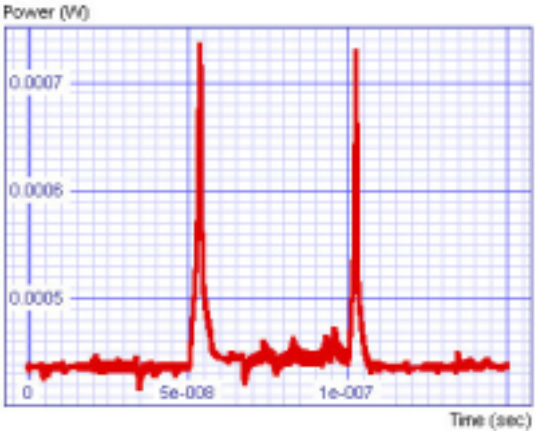
6.3 Comparing Results

According the author's knowledge, the simulation results of the 0.25um CMOS current comparator are better than existing current comparators to date. The performance is based two criteria: delay time and average power consumption. The results are summarized below (Figure 24).

Input



Output: Instantaneous Power



	Results	Lin et al
CMOS technology	0.25 um	0.35 um
Delay for 0.1um input	2.72 ns	2.8 ns
Average Power Consumption	0.45 mW	0.58 mW

Figure 24: Power Consumption for Current Pulse Input and Results Compared

A pulse input is used to measure the average power consumption, as opposed to the PWM test current input, because this is a standard method of measuring power consumption. The graph of the instantaneous power consumption for the pulse input is shown on the bottom-left. In either case, the results for the average power consumed are fairly similar for both inputs.

7.0 Conclusion

As a research intern of Polytechnic University's Electrical and Computer Engineering (ECE) Department's 2002 Summer Research Program, the author had the opportunity to work on a project aimed at reducing power consumption in mobile wireless communication devices. With the understanding that the power amplifier consumes the majority of power in a transceiver, the author designed a component of a converter controller that will be placed into the power amplifier to minimize its power consumption, specifically the RF dc-dc current comparator. A new current comparator design is proposed, along with a specific design methodology that can be carried across different technologies. The final results are two current comparators, one designed in 0.5um CMOS technology and the other in 0.25um CMOS technology, with the latter design performing better than any published designs to the author's knowledge.

The author would like to thank James Masciotti, who is a graduate M.S. student of Polytechnic University's ECE Department, for his extensive help with the research. The author would especially like to thank his advisor Professor Dariusz Czarkowski, who is a professor at Polytechnic University's ECE Department, for his advice and assistance.

8.0 Appendix A

SPICE Parameters

0.25um CMOS Current Comparator

```
*Current Amplifier
M1 1 1 3 3      CMOSP w=.36u l=.48u ps=3.96u pd=3.96u
M2 1 1 4 4      CMOSN w=.36u l=2.04u ps=3.96u pd=3.96u
M3 5 1 15 15    CMOSP w=.36u l=.24u ps=3.96u pd=3.96u
M4 5 1 4 4      CMOSN w=.36u l=.6u ps=3.96u pd=3.96u
Rp 15 3 124.9

*Inverter 1
M5 6 5 3 3      CMOSP w=1.08u l=.24u ps=4.68u pd=4.68u
M6 6 5 4 4      CMOSN w=.36u l=.24u ps=3.96u pd=3.96u

*Output Stage
M7 3 6 5 5      CMOSN w=.36u l=.24u ps=3.96u pd=3.96u
M8 4 6 5 5      CMOSP w=.36u l=.24u ps=3.96u pd=3.96u

*Inverter 2
M9 14 6 3 3     CMOSP w=1.08u l=.24u ps=4.68u pd=4.68u
M10 14 6 4 4    CMOSN w=.36u l=.24u ps=3.96u pd=3.96u

*Inverter 3
M11 2 14 3 3    CMOSP w=1.08u l=.24u ps=4.68u pd=4.68u
M12 2 14 4 4    CMOSN w=.36u l=.24u ps=3.96u pd=3.96u

Vss 3 0 1.25
Vdd 4 0 -1.25

V1 20 0 dc 0 PWL (0 -.1u 50n -.1u 50.001n .1u 100n .1u 100.001n -.1u 150 -.1u)
Gs 0 1 20 0 1

.MODEL CMOSN NMOS (                     LEVEL   = 7
+TNOM    = 27           TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3731371
+K1      = 0.4626989    K2      = 3.610998E-3   K3      = 1E-3
+K3B     = 3.4473437    W0      = 1E-7          NLX     = 2.161822E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.465353     DVT1    = 0.4682776     DVT2    = -0.3600181
+U0      = 291.8807271  UA      = -1.358982E-9  UB      = 2.600205E-18
+UC      = 3.68755E-11  VSAT    = 1.453872E5    A0      = 1.7973899
```

```
+AGS     = 0.3280843      B0      = -1.492756E-7   B1      = 5.826141E-7
+KETA    = -7.07971E-3    A1      = 5.600633E-4    A2      = 0.4445546
+RDSW    = 186.5665001    PRWG    = 0.5            PRWB    = -0.2
+WR      = 1              WINT    = 0              LINT    = 0
+DWG     = -1.627919E-8
+DWB     = 2.793508E-9    VOFF    = -0.0951886     NFACTOR = 1.5570816
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 4.389028E-3    ETAB    = 4.381099E-4
+DSUB    = 0.0217698      PCLM    = 1.679854       PDIBLC1 = 0.4416943
+PDIBLC2 = 2.720463E-3    PDIBLCB = -0.1           DROUT   = 0.7370237
+PSCBE1  = 6.82413E8      PSCBE2  = 5E-10          PVAG    = 0
+DELTA   = 0.01           RSH     = 4.6            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 5.72E-10       CGSO    = 5.72E-10       CGBO    = 1E-12
+CJ      = 1.730461E-3    PB      = 0.9837155      MJ      = 0.4592833
+CJSW    = 4.058445E-10   PBSW    = 0.99           MJSW    = 0.3212178
+CJSWG   = 3.29E-10       PBSWG   = 0.99           MJSWG   = 0.3212178
+CF      = 0              PVTH0   = -0.01          PRDSW   = -10
+PK2     = 2.212933E-3    WKETA   = 7.871804E-3    LKETA   = -4.438935E-3    )
*
.MODEL CMOSP PMOS (                               LEVEL   = 7
+TNOM    = 27             TOX     = 5.7E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.5502511
+K1      = 0.6400201      K2      = -1.704113E-3   K3      = 0
+K3B     = 15.9111313     W0      = 1E-6           NLX     = 1.607639E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.7644417      DVT1    = 0.8479803      DVT2    = -0.1546672
+U0      = 105.2755214    UA      = 1.186284E-9    UB      = 1.176835E-21
+UC      = -1E-10         VSAT    = 2E5            A0      = 0.9791315
+AGS     = 0.1953302      B0      = 1.093685E-6    B1      = 5E-6
+KETA    = 0.0143725      A1      = 2.376941E-3    A2      = 0.3
+RDSW    = 774.3628818    PRWG    = 0.5            PRWB    = -0.3137681
+WR      = 1              WINT    = 0              LINT    = 3.367961E-8
+DWG     = -4.703854E-8
+DWB     = 4.628024E-9    VOFF    = -0.1352255     NFACTOR = 0.9595714
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.9487547      ETAB    = -0.5
+DSUB    = 1.327526       PCLM    = 1.2246157      PDIBLC1 = 4.978793E-3
+PDIBLC2 = -1.067618E-8   PDIBLCB = -1E-3          DROUT   = 0.0589797
+PSCBE1  = 6.155146E9     PSCBE2  = 5.00025E-10    PVAG    = 2.250493E-6
```

```
+DELTA   = 0.01          RSH     = 3.4           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 6.76E-10      CGSO    = 6.76E-10      CGBO    = 1E-12
+CJ      = 1.906078E-3   PB      = 0.99          MJ      = 0.4662316
+CJSW    = 3.337172E-10  PBSW    = 0.6541995     MJSW    = 0.3130577
+CJSWG   = 2.5E-10       PBSWG   = 0.6541995     MJSWG   = 0.3130577
+CF      = 0             PVTH0   = 7.047217E-3   PRDSW   = 3.0435715
+PK2     = 3.077599E-3   WKETA   = 0.033745      LKETA   = -9.457104E-3   )
.end
```

9.0 References

[1] J.M. Masciotti, "CMOS Current Conveyor for RF Dc-Dc Converter Controllers", Polytechnic University, NY, 2002.

[2] Prism Technical Information. http://www.intersil.com/design/prism/wirelessb.asp

[3] J. Biernacki, and D. Czarkowski, "Radio Frequency DC-DC Flyback Converter", *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems (MWSCAS'2000)*, Vol. 1, pp. 94-97

[4] D.W. Hart, "Introduction to Power Electronics", Prentice Hall, NJ, 1997, Chap. 6.

[5] H. Lin, J. Huang, S. Wong, "A Simple High-Speed Low Current Comparator", *IEEE Intl. Symposium on Circuits and Systems ISCAS'2000*, Geneva, Vol. 2 pp. 713-716

[6] L. Chen, B. Shi, and C. Lu, "A Robust High-speed and Low-power CMOS Current Comparator Circuit", Tsinghua University, Beijing, 2002.

[7] MOSIS, http://www.mosis.org